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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	MI22-1322
First Inventor or Application Identifier	Vishnu K. Agarwal
Title	Integrated Circuitry And Method Of Forming A Capacitor
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jc525 U.S. PTO 09/511140 02/23/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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   - Descriptive title of the Invention PLUS TITLE PAGE
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
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7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
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17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 021567 *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name	Mark S. Matkin				
	Wells, St. John, Roberts, Gregory & Matkin P.S.				
Address	W. 601 First Ave., Suite 1300				
City	Spokane	State	WA	Zip Code	99201-3828
Country		Telephone	(509) 624-4276	Fax	(509) 838-3424

Name (Print/Type)	Mark S. Matkin	Registration No. (Attorney/Agent)	32,268
Signature	Mark S. Matkin	Date	2-23-00

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EL465677919

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Integrated Circuitry And Method Of Forming A Capacitor

* * * * *

INVENTOR

Vishnu K. Agarwal

ATTORNEY'S DOCKET NO. MI22-1322

Integrated Circuitry And Method Of Forming A Capacitor

TECHNICAL FIELD

This invention relates to integrated circuitry and to methods of forming capacitors.

BACKGROUND OF THE INVENTION

As DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell area. Additionally, there is a continuing goal to further decrease cell area. One principal way of increasing cell capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors, such as trenched or stacked capacitors. Yet as feature size continues to become smaller and smaller, development of improved materials for cell dielectrics as well as the cell structure are important. The feature size of 256Mb DRAMs and beyond will be on the order of 0.25 micron or less, and conventional dielectrics such as SiO_2 and Si_3N_4 might not be suitable because of small dielectric constants.

Highly integrated memory devices, such as 256 Mbit DRAMs and beyond, are expected to require a very thin dielectric film for the 3-dimensional capacitor of cylindrically stacked or trench structures. To meet this requirement, the capacitor dielectric film thickness will be below 2.5nm of SiO_2 equivalent thickness.

Insulating inorganic metal oxide materials (such as ferroelectric materials, perovskite materials and pentoxides) are commonly referred to as "high K" materials due to their high dielectric constants, which make them attractive as dielectric materials in capacitors, for example for high density DRAMs and non-volatile memories. In the context of this document, "high K" means a material having a dielectric constant of at least 10. Such materials include tantalum pentoxide, barium strontium titanate, strontium titanate, barium titanate, lead zirconium titanate and strontium bismuth titanate. Using such materials might enable the creation of much smaller and simpler capacitor structures for a given stored charge requirement, enabling the packing density dictated by future circuit design.

Despite the advantages of high dielectric constants and low leakage, insulating inorganic metal oxide materials suffer from many drawbacks. For example, all of these materials incorporate oxygen or are otherwise exposed to oxygen for densification to produce the desired capacitor dielectric layer. Densification or other exposure to an oxygen containing environment is utilized to fill oxygen vacancies which develop in the material during its formation. For example when depositing barium strontium titanate, the material as-deposited can have missing oxygen atoms that may deform its crystalline structure and yield poor dielectric properties. To overcome this drawback, for example, the material is typically subjected to a high temperature anneal in the presence of an oxygen ambient. The anneal drives any carbon present out of the layer and advantageously injects additional oxygen into the layer such that the layer uniformly approaches a stoichiometry

of five oxygen atoms for every two tantalum atoms. The oxygen anneal is commonly conducted at a temperature of from about 400° C to about 1000° C utilizing one or more of O_3, N_2O and O_2. The oxygen containing gas is typically flowed through a reactor at a rate of from about 0.5 slm to about 10 slm.

Certain high K dielectric materials have better current leakage characteristics in capacitors than other high K dielectric materials. In some materials, aspects of a high K material which might be modified or tailored to achieve a highest capacitor dielectric constant possible but will unfortunately also tend to hurt the leakage characteristics (i.e., increase current leakage). One method of decreasing leakage while maximizing capacitance is to increase the thickness of the dielectric region in the capacitor. Unfortunately, this is not always desirable.

SUMMARY

The invention comprises integrated circuitry and methods of forming capacitors. In one implementation, integrated circuitry includes a capacitor having a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween. The high K capacitor dielectric region has a high K substantially amorphous material layer and a high K substantially crystalline material layer. In one implementation, a capacitor forming method includes forming a first capacitor electrode layer over a substrate. A substantially amorphous first high K capacitor dielectric material layer is deposited over the first capacitor electrode layer. The substantially amorphous high K first capacitor dielectric material layer is converted to be substantially crystalline. After the converting, a substantially amorphous second high K capacitor dielectric material layer is deposited over the substantially crystalline first high K capacitor dielectric material layer. A second capacitor electrode layer is formed over the substantially amorphous second high K capacitor dielectric material layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a view of a semiconductor wafer fragment comprising integrated circuitry in accordance with an aspect of the invention.

Fig. 2 is a view of an alternate embodiment semiconductor wafer fragment comprising integrated circuitry in accordance with an aspect of the invention.

Fig. 3 is a view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 4 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that depicted by Fig. 3.

Fig. 5 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that depicted by Fig. 4.

Fig. 6 is a diagrammatic depiction of one preferred processing flow in accordance with an aspect of the invention.

Fig. 7 is a diagrammatic depiction of another preferred processing flow in accordance with an aspect of the invention.

Fig. 8 is a diagrammatic depiction of still another preferred processing flow in accordance with an aspect of the invention.

Fig. 9 is a diagrammatic depiction of example integrated circuitry in accordance with an aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

It is recognized that high K crystalline dielectric materials tend to have higher dielectric constant than high K amorphous dielectric materials. For example, amorphous Ta_2O_5 dielectric constants range from 15 to 20, while the dielectric constants of crystalline Ta_2O_5 can range from 35 to 45. Yet, leakage characteristics of crystalline Ta_2O_5 are much worse than amorphous Ta_2O_5, and thus could potentially limit the use of crystalline Ta_2O_5. However, it would be desirable to take advantage of higher dielectric constants of, for example, crystalline Ta_2O_5 as capacitor area continues to shrink.

A first embodiment example integrated circuitry in accordance with but one aspect of the invention is depicted in Fig. 1. Such comprises a semiconductor wafer fragment 10 comprising a semiconductor substrate 12 and overlying insulative layer 14, such as silicon dioxide. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate region 12 in this example preferably comprises bulk monocrystalline silicon,

although other materials and semiconductor-on-insulator constructions are, of course, contemplated. Discussion proceeds with description of a capacitor construction 17 fabricated over substrate 12/14.

A first capacitor electrode layer 16 is formed over substrate 12/14. Such could comprise any suitable conductive material, with inherently conductive metals such as elemental metals and metal alloys, and conductive metal oxides, and mixtures thereof being preferred. An exemplary thickness range for electrode layer 16 is from about 100 Angstroms to about 1000 Angstroms.

A high K capacitor dielectric region 20 is formed over first capacitor electrode layer 16. A second capacitor electrode layer 30, preferably the same as the first, is formed over high K capacitor dielectric region 20, such that high K capacitor dielectric region 20 is received between electrode layers 16 and 30. High K capacitor dielectric region 20 comprises a high K substantially crystalline material layer 22 and a high K substantially amorphous material layer 24. In the context of this document, "substantially crystalline" means greater than or equal to about 70% crystallinity, whereas "substantially amorphous" means that the subject material layer is greater than or equal to about 70% amorphous phase. More preferably the substantially crystalline and substantially amorphous materials have greater than 90%, and more preferably greater than 98% of their respective phase. A preferred thickness range for layers 22 and 24 is from about 20 Angstroms to about 250 Angstroms each. A preferred thickness range for capacitor dielectric region 20 is from about 40 Angstroms to about 500 Angstroms, with such region preferably being the

only capacitor dielectric region which is received between first capacitor electrode 16 and second capacitor electrode 30. Accordingly preferably, high K capacitor dielectric region 20 consists essentially of high K substantially amorphous material layer 24 and high K substantially crystalline material layer 22.

The high K substantially amorphous material and the high K substantially crystalline material may constitute the same chemical composition, or different chemical compositions. For example, and by way of example only, layer 22 might comprise or consist essentially of barium strontium titanate, while layer 24 might comprise or consist essentially of Ta_2O_5. Most preferably, layers 22 and 24 comprise the same chemical composition, with a preferred material being Ta_2O_5, but for a phase difference in the material as described above and subsequently below. Other dielectric materials might also, of course, be received within capacitor dielectric region 20, but such is not most preferred. Further, more than the illustrated two amorphous and crystalline layers might be received there.

Further preferably, at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and second capacitor electrode. Further preferably, the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode. Further preferably, the high K capacitor substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode. As shown, the high K substantially amorphous material layer

contacts one of the first and second capacitor electrodes (electrode 30 as shown), and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes (electrode 16 as shown). Thus in the Fig. 1 depicted embodiment, capacitor 17 is received at least partially over semiconductor substrate 12, with the high K substantially crystalline material layer 22 being received between semiconductor substrate 12 and high K substantially amorphous material layer 24.

Fig. 2 depicts an alternate embodiment wherein the positionings of layer 22 and 24 have been reversed. Like numerals from the first described embodiment are utilized where appropriate, with differences being indicated with the suffix "a".

The subject capacitors might be fabricated in any of a number of ways. Some example embodiments are described with reference to Figs. 3-8, and with reference to the Fig. 1 preferred embodiment. Like numerals from the first described embodiment are utilized where appropriate, with differences being depicted with different numerals. Referring initially to Figs. 3 and 6, a substantially amorphous first high K capacitor dielectric material layer 21 is formed over first capacitor electrode layer 16, and preferably to contact electrode layer 16 as shown. Such is preferably deposited to the same thickness as layer 22 in the Fig. 1 embodiment. Ta_2O_5 is the preferred material, although other substantially amorphous high K materials are of course contemplated. Any existing or yet-to-be-developed technique for forming such amorphous layer can be utilized, with no one in particular being preferred.

Referring to Figs. 4 and 6, substantially amorphous high K first capacitor dielectric material layer 21 (not shown) is converted to be substantially crystalline, as depicted with numeral 22. A preferred technique for doing so comprises an anneal in an inert atmosphere, such as N_2 or Ar, at a temperature from about 650°C to about 950°C at from about 5 Torr to about 1 atmosphere from about one minute to about one hour. Accordingly preferably, the converting occurs in an atmosphere which is substantially void of oxygen.

Referring to Figs. 5 and 6, and after the converting, substantially amorphous second high K capacitor dielectric material layer 24 is formed over substantially crystalline first high K capacitor dielectric material layer 22. Preferably and as shown, layer 24 is formed to physically contact layer 22.

Then preferably, second high K capacitor dielectric material layer 24 is oxidize annealed in an oxygen containing atmosphere at a temperature of no greater than about 600°C, and more preferably from about 300°C to about 550°C, and effective to maintain second high K capacitor dielectric material layer 24 substantially amorphous. Preferred annealing gases include, by way of example only, N_2O, O_2, O_3, and mixtures thereof. Preferred pressure range is from 150 mTorr to 1 atmosphere, and at a time period preferably ranging from about 10 seconds to about 1 hour. Such oxidize annealing preferably densifies and inserts oxygen in layer 24, and also into crystalline layer 22.

Referring to Fig. 1, second capacitor electrode layer 30 is formed over substantially amorphous second high K capacitor dielectric material layer 24, and preferably in physical contact therewith.

Any of a myriad of alternate processing sequences might be performed, with two such sequences being depicted in Figs. 7 and 8. Fig. 7 depicts conducting an oxidize annealing, preferably as described above, intermediate the first deposition of a substantially amorphous high K capacitor dielectric material layer and subsequent crystallization thereof. Fig. 8 depicts exemplary alternate processing whereby an oxidization anneal is conducted intermediate crystallization of the first substantially amorphous deposited high K capacitor dielectric layer and the deposit of the second substantially amorphous substantially high K dielectric layer.

Such integrated circuitry construction and fabrication methods might be used in a number of different applications, by way of example only in the fabrication of logic or memory circuitry, such as DRAM circuitry fabrication. Fig. 9 illustrates DRAM circuitry and fabrication thereof. A wafer fragment 110 comprises a bulk monocrystalline silicon substrate 112 having a pair of field isolation regions 114. A series of four DRAM word line constructions 116, 117, 118 and 119 are formed over the illustrated substrate, and comprise gates of respective DRAM cell field effect transistors. Gate constructions 116, 117, 118 and 119 are conventional as shown, and comprise a gate dielectric layer (not shown), an overlying conductive polysilicon region, an overlying higher conductive elemental metal or silicide region, and an insulative cap and sidewall spacers, and which are not otherwise specifically

identified with numerals. In the illustrated section, word line 117 comprises a transistor access gate having associated source/drain diffusion regions 120 and 122 formed within monocrystalline silicon substrate 12. Similarly, DRAM word line 118 comprises a gate of a DRAM cell field effect transistor having an associated pair of source/drain diffusion regions 122 and 124. Such depicts two DRAM cells which share a source/drain region 22 which will electrically connect with a bit line, as described subsequently. The other respective source/drain diffusion regions 120 and 24 are formed in electrical connection with DRAM cell capacitor constructions 126 and 127, respectively. The illustrated example is in the fabrication of bit line-over-capacitor DRAM integrated circuitry construction, although other DRAM integrated circuitry and other integrated circuitry constructions and fabrication methods are contemplated.

Conductive covering regions 134 are formed over source/drain regions 120, 122 and 124. Such might be formed to have outermost surfaces or tops which are received elevationally below the outermost top surfaces of gate constructions 116-119 as shown, or received elevationally thereabove (not shown). Such might comprise conductive polysilicon, metals, and/or metal compounds, including conductive barrier layer materials.

An insulating layer 128, for example borophosphosilicate glass (BPSG), is formed over the word lines and is planarized as shown. An antireflective coating layer or layers (not shown) might preferably comprise an outermost portion of layer 128, and comprise silicon oxynitride which can also function as a diffusion barrier to hydrogen and other gases. Capacitor container

openings 130 and 131 are formed within insulative layer 128 over source/drain diffusion regions 120 and 124, respectively, and the associated conductive covering regions 134. A capacitor storage node layer 136 is formed within container openings 130 and 131 in electrical connection with source/drain diffusion regions 120 and 124 through conductive covering/plugging material 134. Such can be planarized back to be isolated within the container openings as shown. Example materials include conductively doped polysilicon, metal and metal compounds, with conductive metal oxides being preferred materials. Example conductive metal oxides include ruthenium oxide, iridium oxide, and rhodium oxide.

A capacitor dielectric layer 138 is formed over storage node electrode layer 136. Layer 138 preferably is fabricated to comprise any of the above capacitor dielectric regions 20, 20a or others as described above. A DRAM capacitor cell electrode layer 140 is formed over capacitor dielectric layer 138. Cell electrode layer 140 is preferably common to multiple capacitors of the DRAM circuitry, and preferably comprises a conductive metal oxide. Layer 140 is patterned as desired and shown to provide an opening therethrough to ultimately achieve bit line electrical connection with shared diffusion region 122 (shown and described below), and to otherwise form a desired circuitry pattern thereof outwardly of the fragment depiction of Fig. 9.

An insulative layer 144 is formed over DRAM capacitor cell electrode layer 140. An example and preferred material is BPSG. A contact opening is formed through insulative layers 144 and 128 for ultimate formation of a conductive bit contact. Conductive material 156 is formed

within the contact opening in electrical connection with DRAM capacitor cell electrode layer 140 and within contact opening 146 in electrical connection with bit contact source/drain diffusion region 122. Conductive material 156 preferably comprises a metal and/or metal compound which is/are capable of oxidizing to a non-conductive metal oxide upon effective exposure to the conductive metal oxide of layer 140. Preferred materials include titanium, titanium nitride, and tungsten, by way of example only. Such layers are deposited and planarized back relative to insulative layer 144 as shown.

A conductive layer 165 is deposited over and in electrical connection with conductive material 156. Such is patterned to form a DRAM bit line 166 over insulative layer 144 and in electrical connection with source/drain diffusion region 122 through conductive material 156. Other devices might be formed outwardly of layer 168, followed ultimately by formation of a final passivation layer.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer.

2. The integrated circuitry of claim 1 wherein the high K substantially amorphous material and the high K substantially crystalline material constitute the same chemical composition.

3. The integrated circuitry of claim 1 wherein the high K substantially amorphous material and the high K substantially crystalline material constitute different chemical compositions.

4. The integrated circuitry of claim 1 wherein at least one of the first and second electrodes comprises elemental metal, metal alloy, conductive metal oxides, or mixtures thereof.

5. The integrated circuitry of claim 1 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

6. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

7. The integrated circuitry of claim 6 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode and the second capacitor electrode.

8. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrodes and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrodes.

9. The integrated circuitry of claim 1 wherein the high K capacitor dielectric region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

10. The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 98% amorphous, and the high K substantially crystalline material layer is at least 98% crystalline.

11. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially crystalline material layer being received between the semiconductor substrate and the high K substantially amorphous material layer.

12. The integrated circuitry of claim 11 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

13. The integrated circuitry of claim 11 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

14. The integrated circuitry of claim 11 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

15. The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially amorphous material layer being received between the semiconductor substrate and the high K substantially crystalline material layer.

16. The integrated circuitry of claim 15 wherein the semiconductor substrate comprising bulk monocrystalline silicon.

17. Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a Ta_2O_5 comprising capacitor dielectric region received therebetween; the Ta_2O_5 comprising region comprising a substantially amorphous Ta_2O_5 comprising layer and a substantially crystalline Ta_2O_5 comprising layer.

18. The integrated circuitry of claim 17 wherein at least one of the substantially amorphous Ta_2O_5 comprising layer and the substantially crystalline Ta_2O_5 comprising layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

19. The integrated circuitry of claim 17 wherein the substantially amorphous Ta_2O_5 comprising layer contacts at least one of the first capacitor electrode and the second capacitor electrode.

20. The integrated circuitry of claim 19 wherein the substantially amorphous Ta_2O_5 comprising layer contacts only one of the first capacitor electrode and the second capacitor electrode.

21. The integrated circuitry of claim 17 wherein the substantially amorphous Ta_2O_5 comprising layer contacts one of the first and second capacitor electrodes and the substantially crystalline Ta_2O_5 comprising layer contacts the other of the first and second capacitor electrodes.

22. The integrated circuitry of claim 17 wherein the Ta_2O_5 comprising region is the only capacitor dielectric region received between the first and second capacitor electrodes, and consists essentially of the substantially amorphous Ta_2O_5 comprising layer and the substantially crystalline Ta_2O_5 comprising layer.

23. A capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

forming a high K capacitor dielectric region over the first capacitor electrode layer, the high K capacitor dielectric region comprising a high K substantially crystalline material layer and a high K substantially amorphous material layer; and

forming a second capacitor electrode layer over the high K capacitor dielectric region.

24. The method of claim 23 comprising forming the high K substantially amorphous material and the high K substantially crystalline material to constitute the same chemical composition.

25. The method of claim 24 wherein the chemical composition comprises Ta_2O_5.

26. The method of claim 23 comprising forming the high K substantially amorphous material and the high K substantially crystalline material to constitute different chemical compositions.

27. The method of claim 23 wherein at least one of the high K substantially amorphous material layer and the high K substantially crystalline material layer contacts at least one of the first capacitor electrode layer and the second capacitor electrode layer.

28. The method of claim 23 wherein the high K substantially amorphous material layer contacts at least one of the first capacitor electrode layer and the second capacitor electrode layer.

29. The method of claim 28 wherein the high K substantially amorphous material layer contacts only one of the first capacitor electrode layer and the second capacitor electrode layer.

30. The method of claim 23 wherein the high K substantially amorphous material layer contacts one of the first and second capacitor electrode layers and the high K substantially crystalline material layer contacts the other of the first and second capacitor electrode layers.

31. The method of claim 23 wherein the high K capacitor dielectric region is formed to be the only capacitor dielectric region received between the first and second capacitor electrode layers, and consists essentially of the high K substantially amorphous material layer and the high K substantially crystalline material layer.

32. The method of claim 23 wherein the high K substantially amorphous material layer is formed to be at least 98% amorphous, and the high K substantially crystalline material layer is formed to be at least 98% crystalline.

33. A capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

34. The method of claim 33 further comprising after the converting and before forming the second capacitor electrode layer, oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous.

35. The method of claim 33 further comprising after the converting and before forming the second capacitor electrode layer, oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of from about 300°C to about 550°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous.

36. The method of claim 33 wherein the converting occurs in an atmosphere which is substantially void oxygen.

37. The method of claim 33 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.

38. The method of claim 37 wherein the chemical composition comprises Ta_2O_5.

39. The method of claim 33 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.

40. The method of claim 33 wherein the second capacitor electrode layer is formed to contact the substantially amorphous second high K capacitor dielectric material layer.

41. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer.

42. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer, and the second capacitor electrode layer is formed to contact the substantially amorphous second high K capacitor dielectric material layer.

43. The method of claim 33 wherein the first high K capacitor dielectric material layer is formed to contact the first capacitor electrode layer, the second high K capacitor dielectric material layer is formed to contact the first high K capacitor dielectric material layer, and the second capacitor electrode layer is formed to contact the second high K capacitor dielectric material layer.

44. A capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

oxidize annealing the first high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C;

after the oxidize annealing of the first high K capacitor dielectric material layer, converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer;

oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

45. The method of claim 44 further wherein the first and second oxidize annealings comprise annealing in an oxygen containing atmosphere at a temperature of no greater than about 600°C.

46. The method of claim 44 wherein the converting occurs in an atmosphere which is substantially void oxygen.

47. The method of claim 44 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.

48. The method of claim 47 wherein the chemical composition comprises Ta_2O_5.

49. The method of claim 44 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.

50. A capacitor forming method comprising:

forming a first capacitor electrode layer over a substrate;

depositing a substantially amorphous first high K capacitor dielectric material layer over the first capacitor electrode layer;

converting the substantially amorphous high K first capacitor dielectric material layer to be substantially crystalline;

after the converting of the substantially amorphous high K first capacitor dielectric material layer, oxidize annealing the first high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C;

after the oxidize annealing of the first high K capacitor dielectric material layer, depositing a substantially amorphous second high K capacitor dielectric material layer over the substantially crystalline first high K capacitor dielectric material layer;

oxidize annealing the second high K capacitor dielectric material layer in an oxygen containing atmosphere at a temperature of no greater than about 600°C and effective to maintain the second high K capacitor dielectric material layer substantially amorphous; and

forming a second capacitor electrode layer over the substantially amorphous second high K capacitor dielectric material layer.

51. The method of claim 50 further wherein the first and second oxidize annealings comprise annealing in an oxygen containing atmosphere at a temperature of no greater than about 600°C.

52. The method of claim 50 wherein the converting occurs in an atmosphere which is substantially void oxygen.

53. The method of claim 50 wherein the first and second dielectric material layers are formed to constitute the same chemical composition.

54. The method of claim 53 wherein the chemical composition comprises Ta_2O_5.

55. The method of claim 50 wherein the first and second dielectric material layers are formed to constitute different chemical compositions.

ABSTRACT OF THE DISCLOSURE

The invention comprises integrated circuitry and to methods of forming capacitors. In one implementation, integrated circuitry includes a capacitor having a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween. The high K capacitor dielectric region has a high K substantially amorphous material layer and a high K substantially crystalline material layer. In one implementation, a capacitor forming method includes forming a first capacitor electrode layer over a substrate. A substantially amorphous first high K capacitor dielectric material layer is deposited over the first capacitor electrode layer. The substantially amorphous high K first capacitor dielectric material layer is converted to be substantially crystalline. After the converting, a substantially amorphous second high K capacitor dielectric material layer is deposited over the substantially crystalline first high K capacitor dielectric material layer. A second capacitor electrode layer is formed over the substantially amorphous second high K capacitor dielectric material layer.

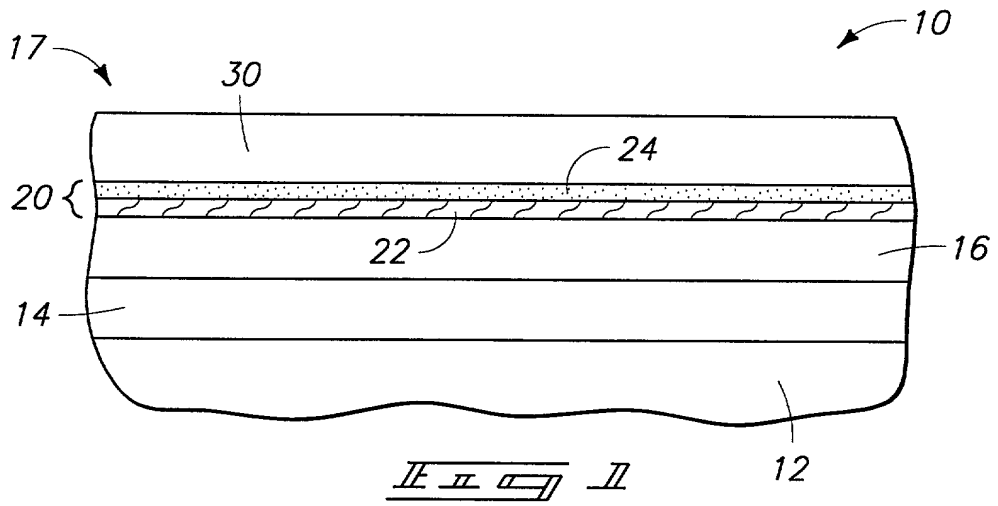

Fig. 1

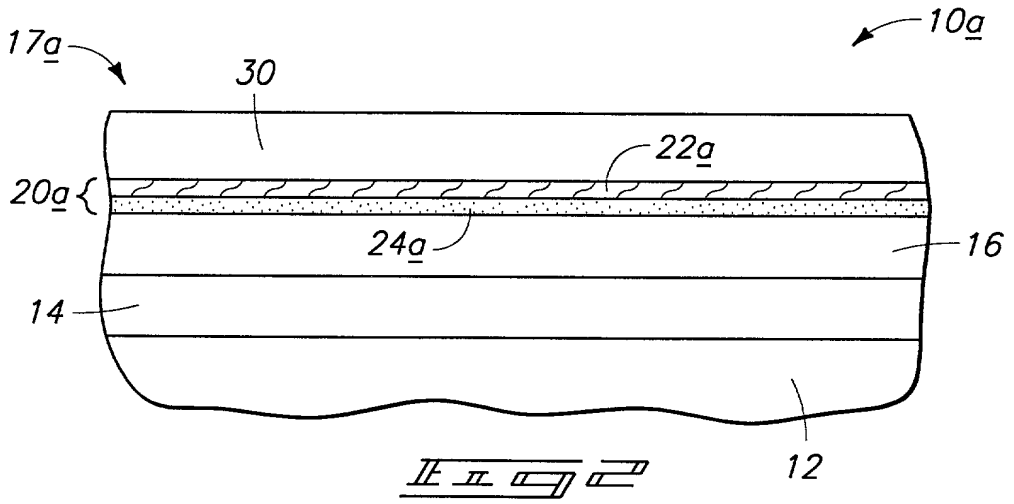

Fig. 2

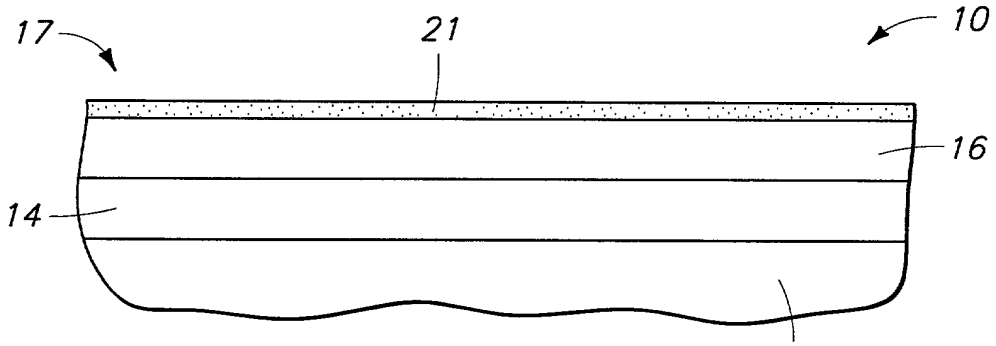

Fig 3

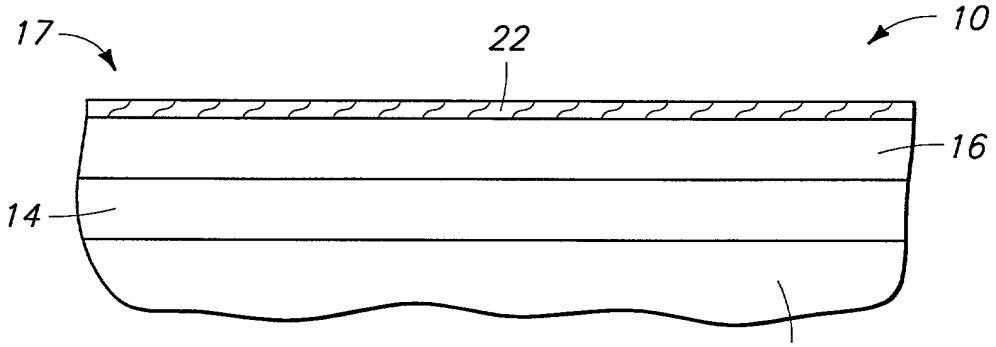

Fig 4

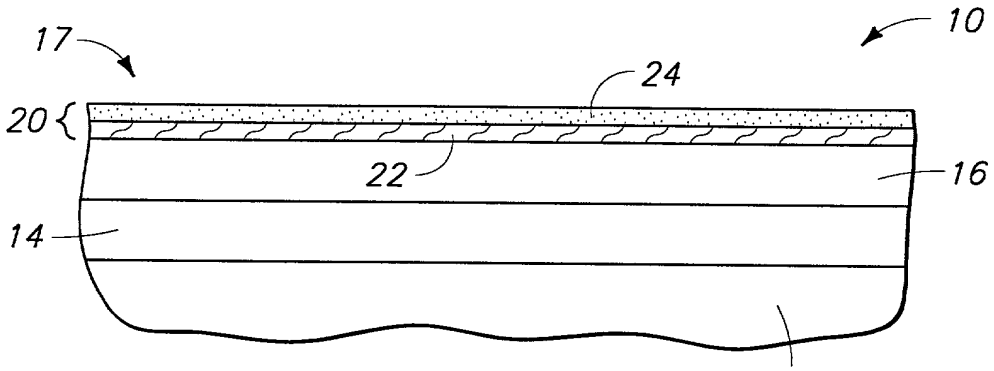
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Fig 5

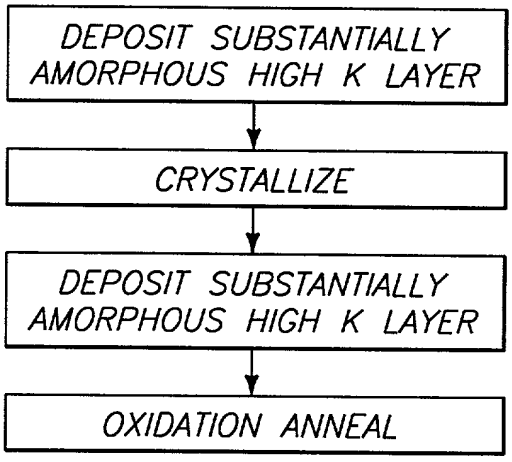
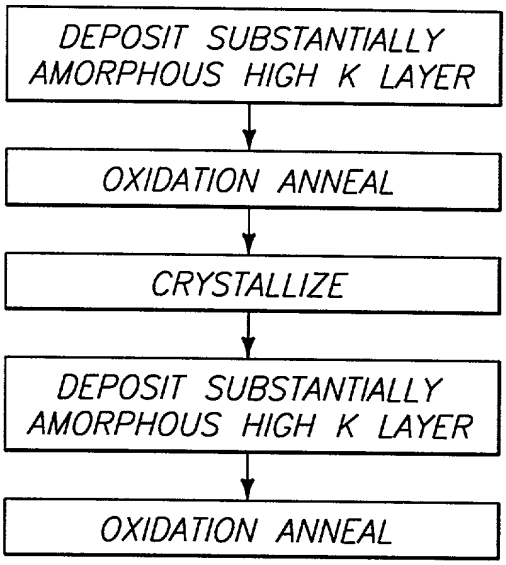

DEPOSIT SUBSTANTIALLY AMORPHOUS HIGH K LAYER
CRYSTALLIZE
DEPOSIT SUBSTANTIALLY AMORPHOUS HIGH K LAYER
OXIDATION ANNEAL

Fig 6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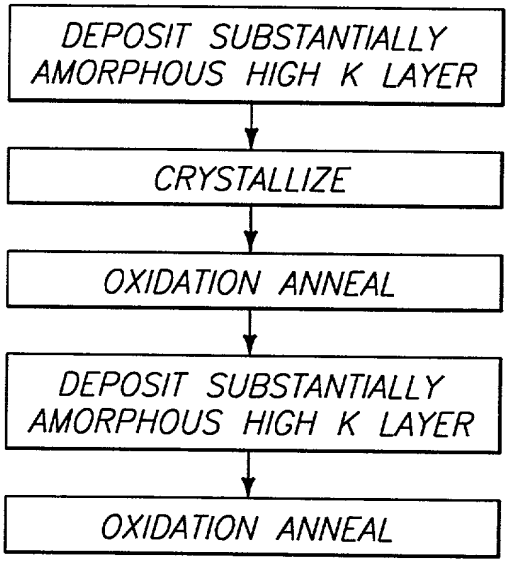
OXIDATION ANNEAL
CRYSTALLIZE
DEPOSIT SUBSTANTIALLY AMORPHOUS HIGH K LAYER
OXIDATION ANNEAL

Fig. 7


DEPOSIT SUBSTANTIALLY AMORPHOUS HIGH K LAYER
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OXIDATION ANNEAL
DEPOSIT SUBSTANTIALLY AMORPHOUS HIGH K LAYER
OXIDATION ANNEAL

Fig. 8

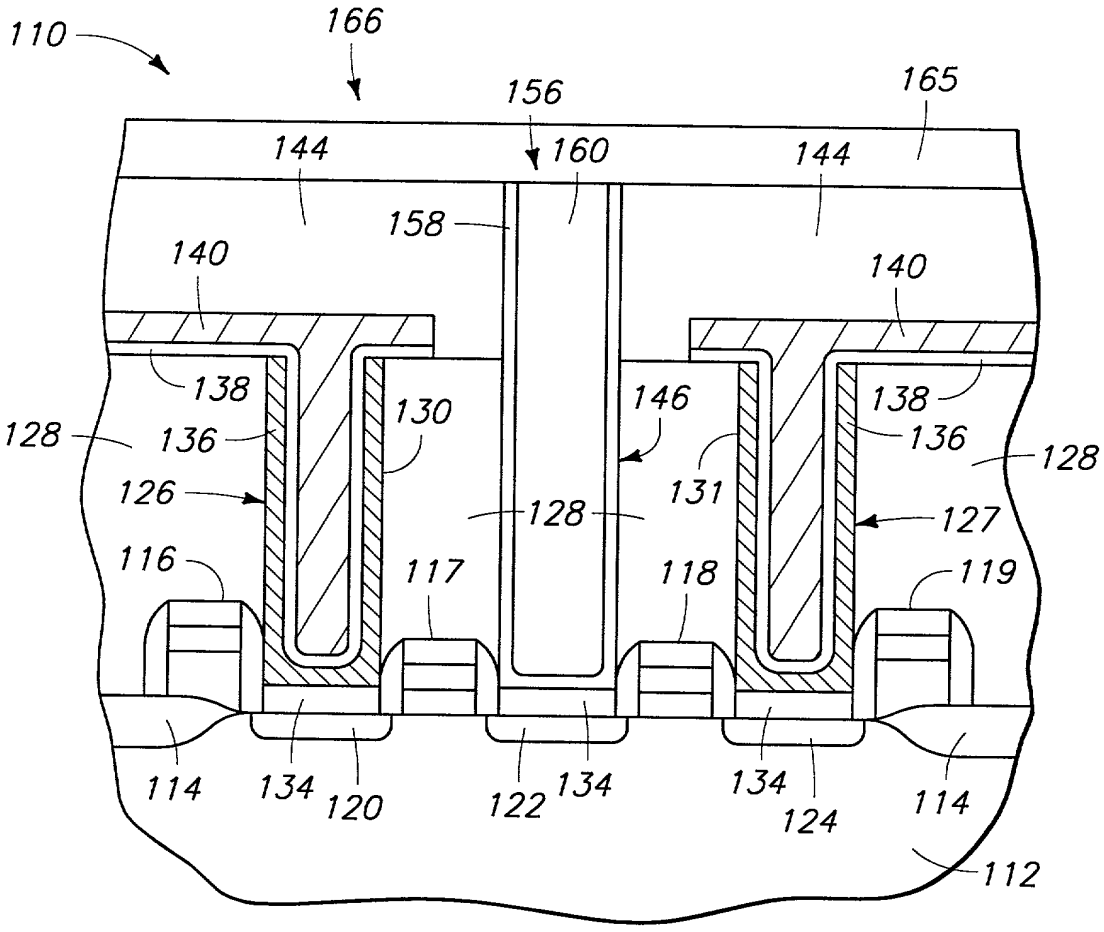
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Fig 9

EL465677919

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **Integrated Circuitry And Method Of Forming A Capacitor**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of sole inventor: **Vishnu K. Agarwal**

Inventor's Signature: _____

Date: 10th February, 2000

Residence: **Boise, Idaho**

Citizenship: **India**

Post Office Address: **2463 E. Red Cedar Lane, #103**
Boise, ID 83716

EL465677919

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. ..... Filed Herewith
Filing Date ..... Filed Herewith
Inventor ..... Vishnu K. Agarwal
Assignee ..... Micron Technology, Inc.
Group Art Unit ..... Unassigned
Examiner ..... Unassigned
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry And Method Of Forming A Capacitor

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right, title and interest in the above-identified patent application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of WELLS, ST. JOHN, ROBERTS, GREGORY & MATKIN P.S., listed as follows:

Richard J. St. John	Reg. No. 19,363
David P. Roberts	Reg. No. 23,032
Randy A. Gregory	Reg. No. 30,386
Mark S. Matkin	Reg. No. 32,268
James L. Price	Reg. No. 27,376
Deepak Malhotra	Reg. No. 33,560
Mark W. Hendricksen	Reg. No. 32,356
David G. Latwesen	Reg. No. 38,533
George G. Grigel	Reg. No. 31,166
Keith D. Grzelak	Reg. No. 37,144
James D. Shaurette	Reg. No. 39,833
Frederick M. Fliegel	Reg. No. 36,138
Donald Brent Kenady	Reg. No. 40,045
James E. Lake	Reg. No. 44,854
Bernard Berman	Reg. No. 37,279

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia Pappas Dennison (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The Assignee certifies that the above-identified Assignment has been reviewed and to the best of Assignee's knowledge and belief, title is in the Assignee, and a copy of the Assignment is submitted herewith.

Please direct all correspondence regarding this application to:

Customer No. 021567
Wells, St. John, Roberts, Gregory & Matkin P.S.
Attn: Mark S. Matkin
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Telephone: (509) 624-4276
Facsimile: (509) 838-3424

MICRON TECHNOLOGY, INC.

Dated: 2-17-00 By: _____

Name: Michael L. Lynch, Esq.
Title: Chief Patent Counsel

Attachment: *Copy of Assignment; Copy of Board of Directors' Resolution*